EE 434

Lecture 34

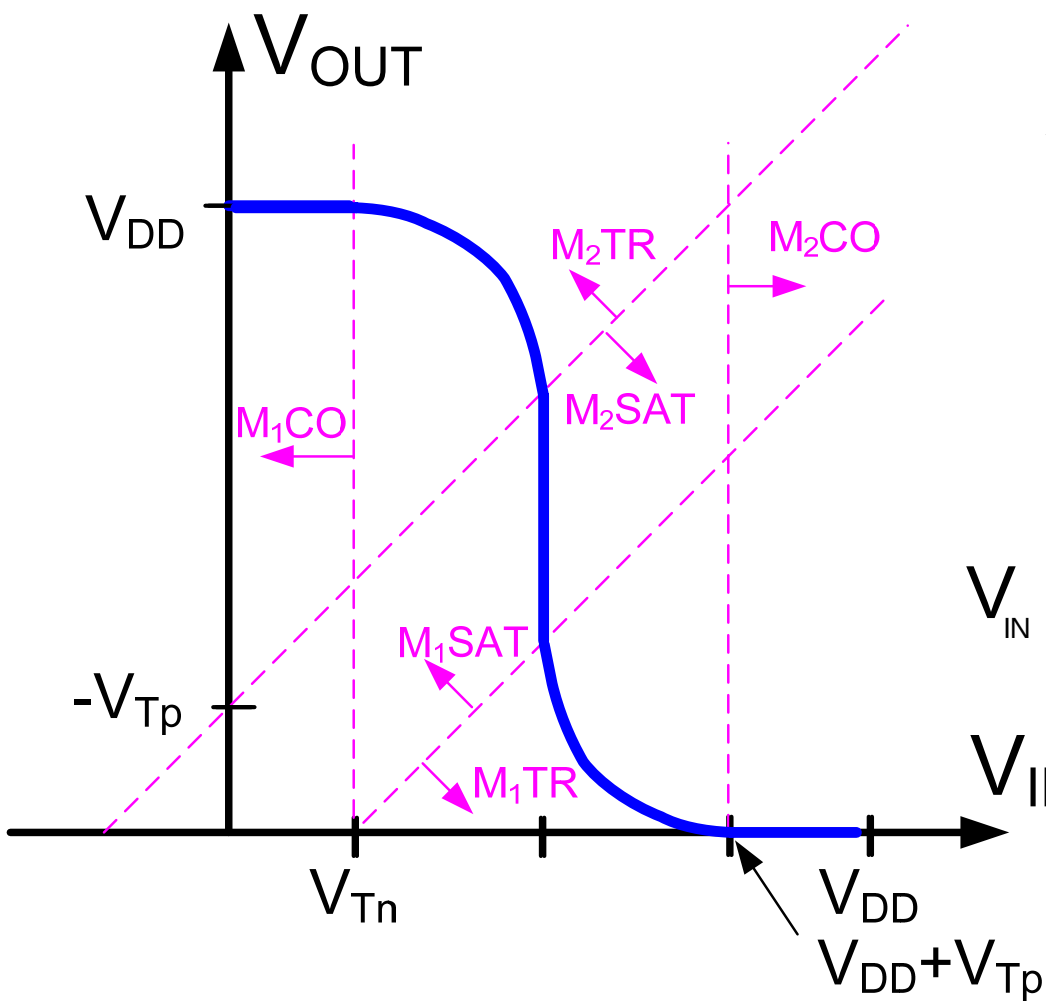
Logic Design

Review from last time:

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 5 M_1 cutoff, M_2 triode



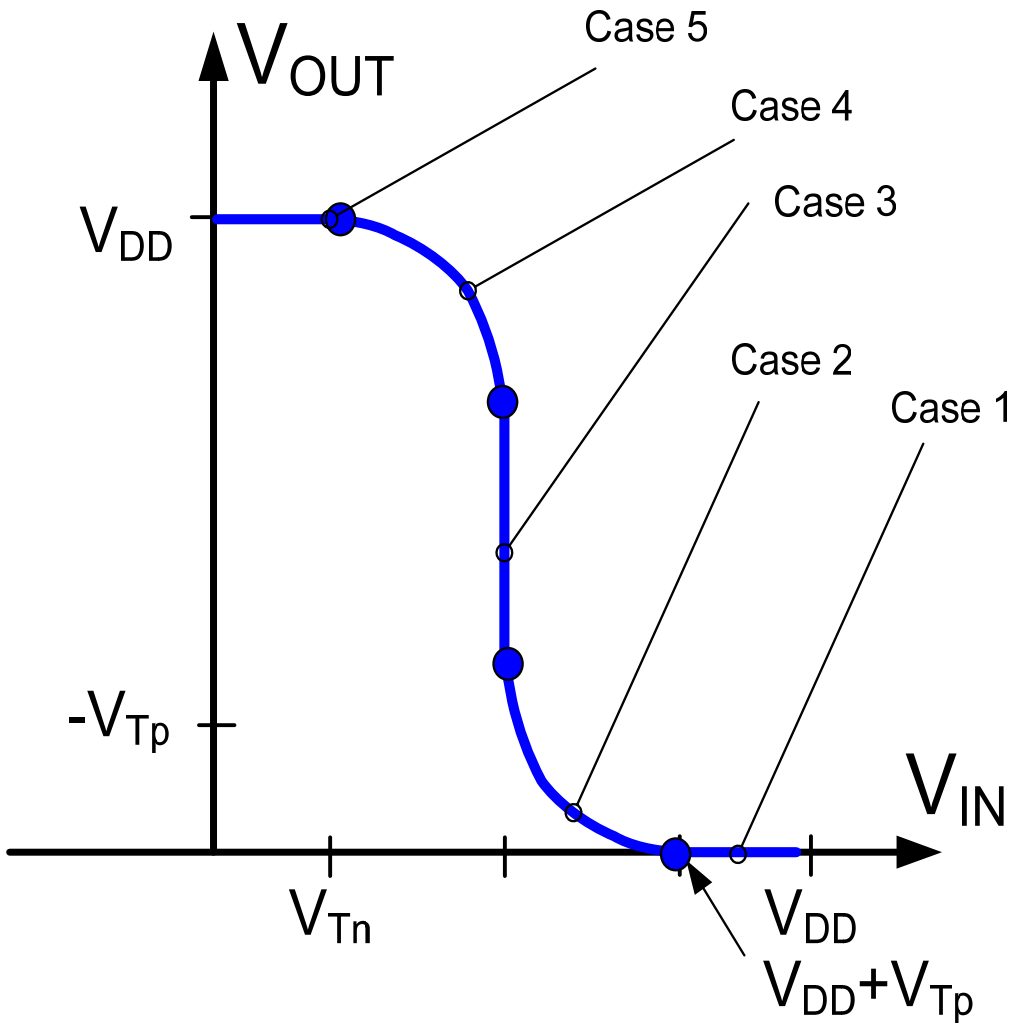
$$V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_{Tp}$$

$$V_{IN} < V_{Tn}$$

$$V_{IN} - V_{DD} \leq V_{Tp}$$

Transfer characteristics of the static CMOS inverter

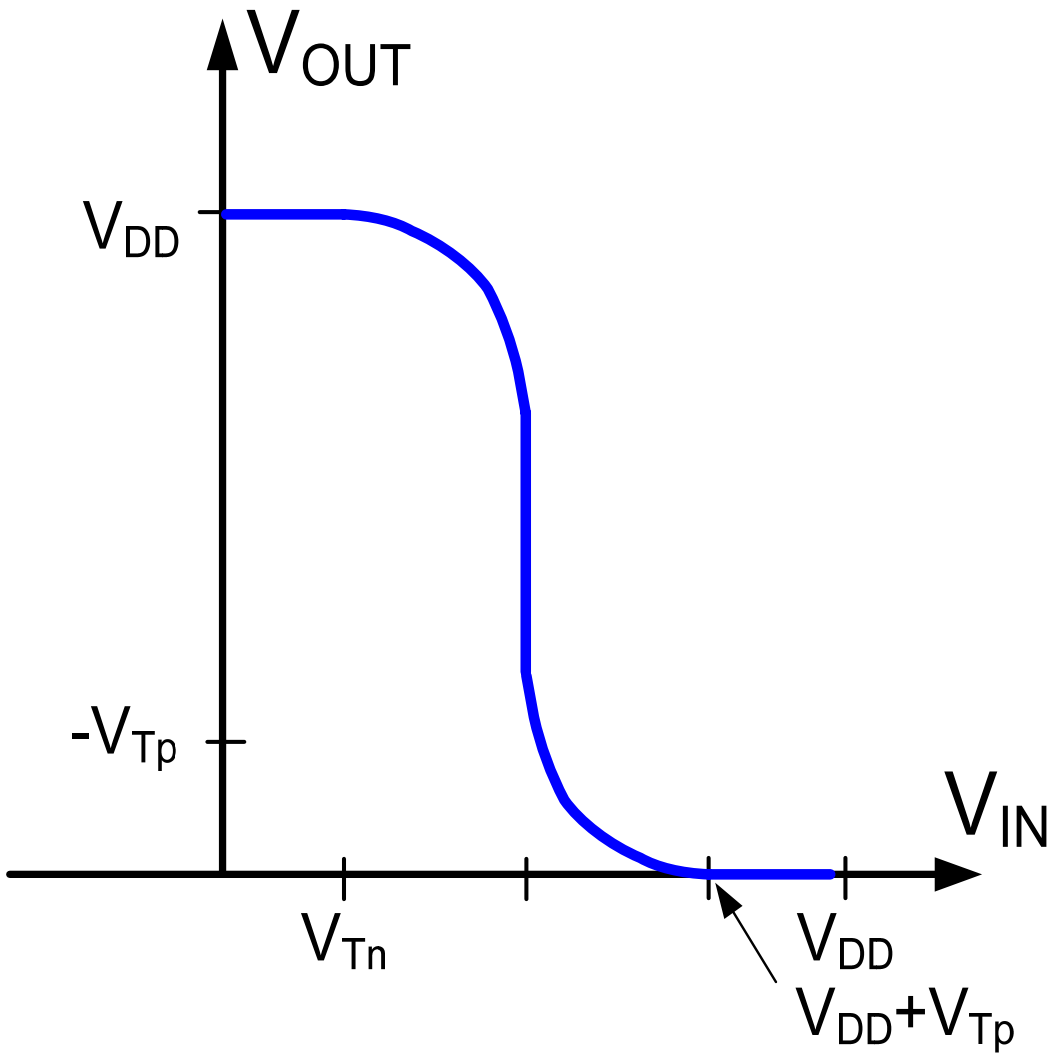
(Neglect λ effects)



Review from last time:

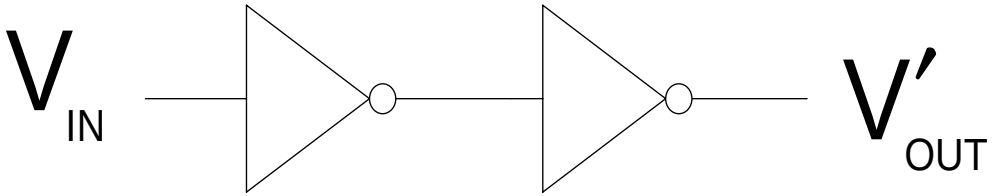
Transfer characteristics of the static CMOS inverter

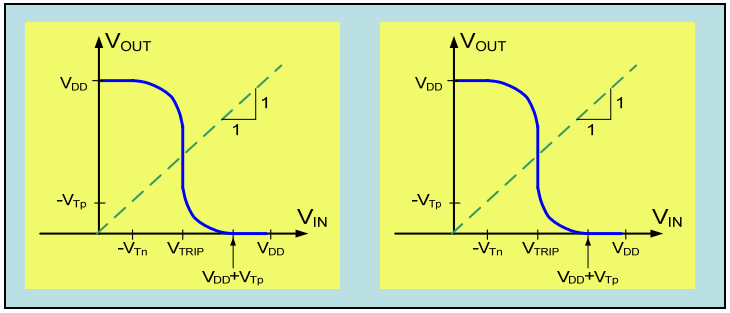
(Neglect λ effects)

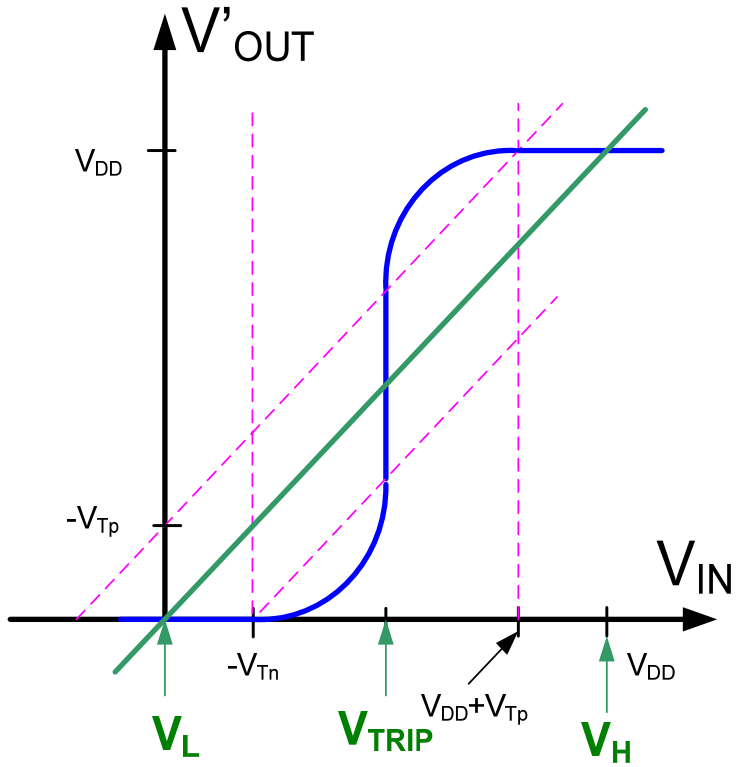


Review from last time:

Inverter Transfer Characteristics of Inverter Pair

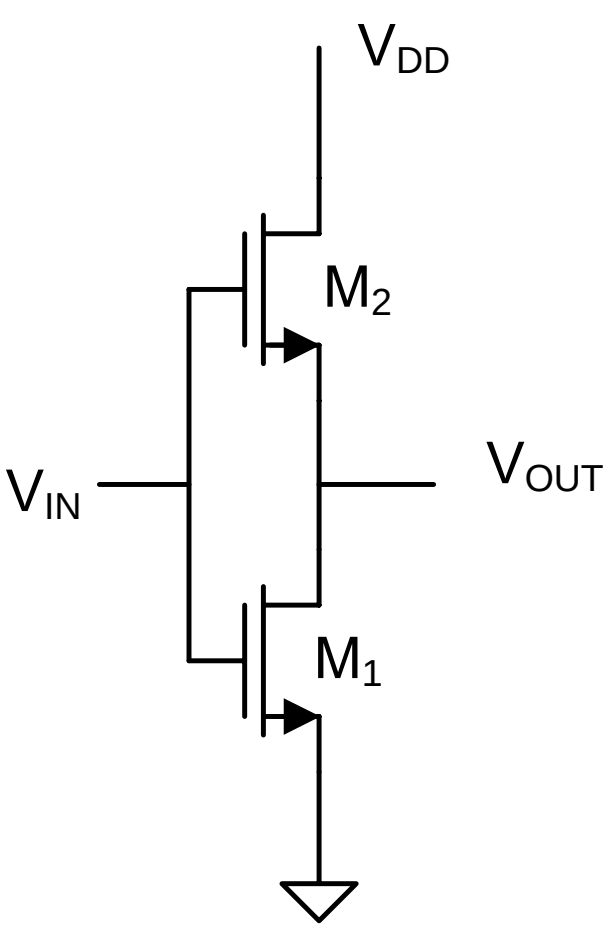


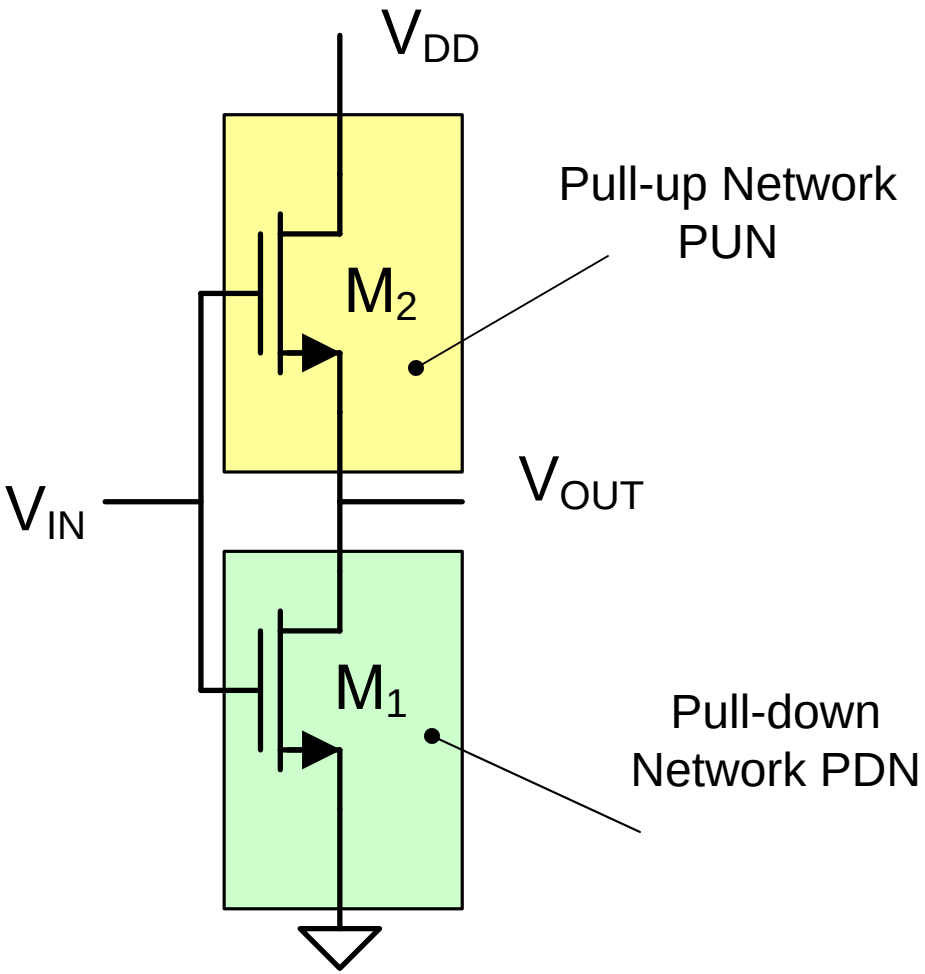




Review from last time:

Static CMOS Logic Family

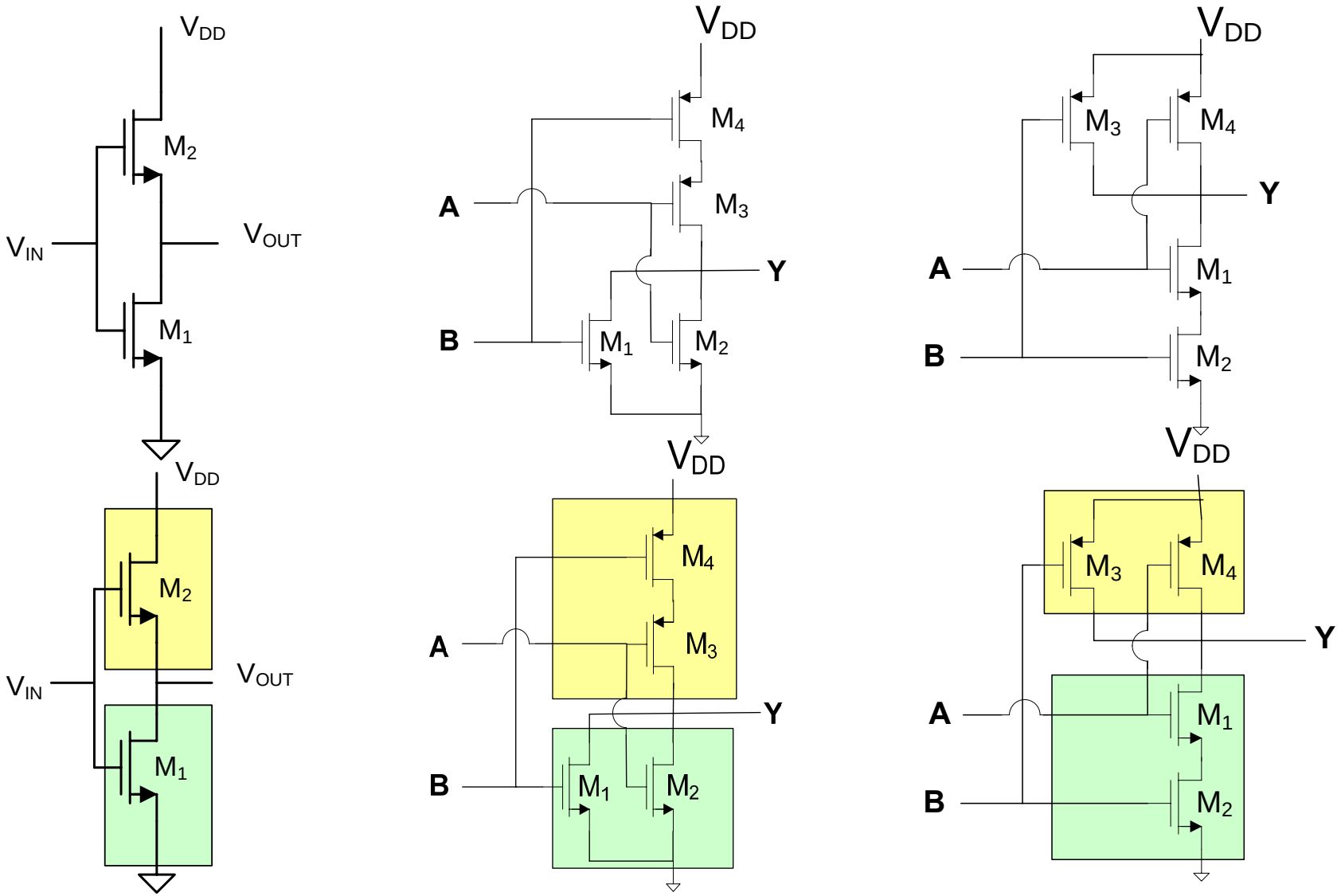




Observe PUN is p-channel, PDN is n-channel

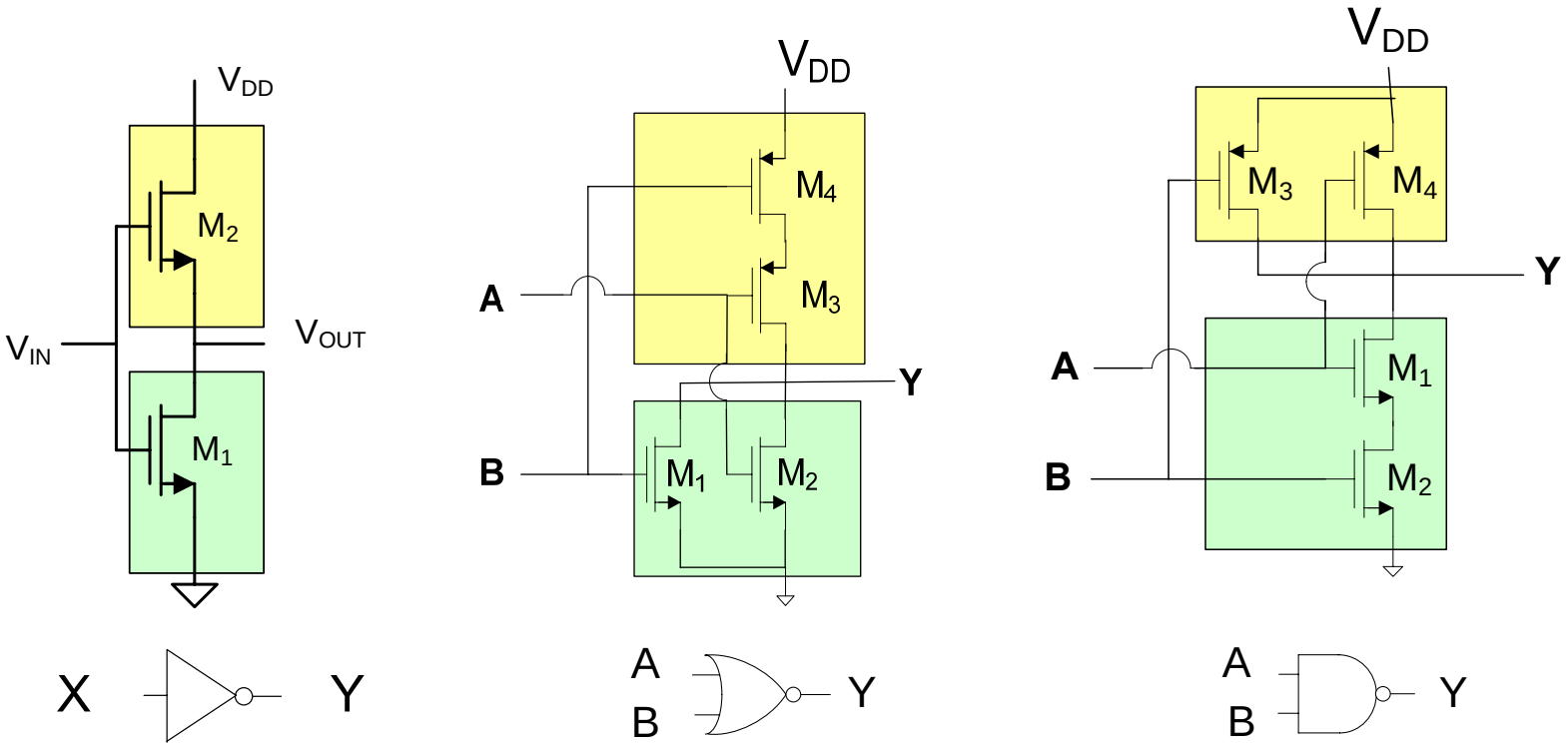
Review from last time:

Static CMOS Logic Family



n-channel PDN and p-channel PUN

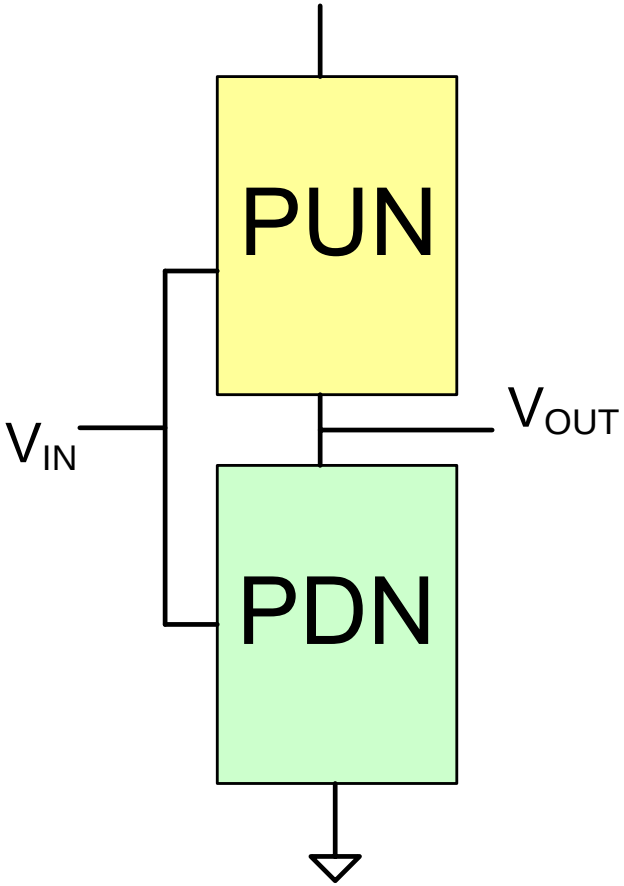
Static CMOS Logic Family



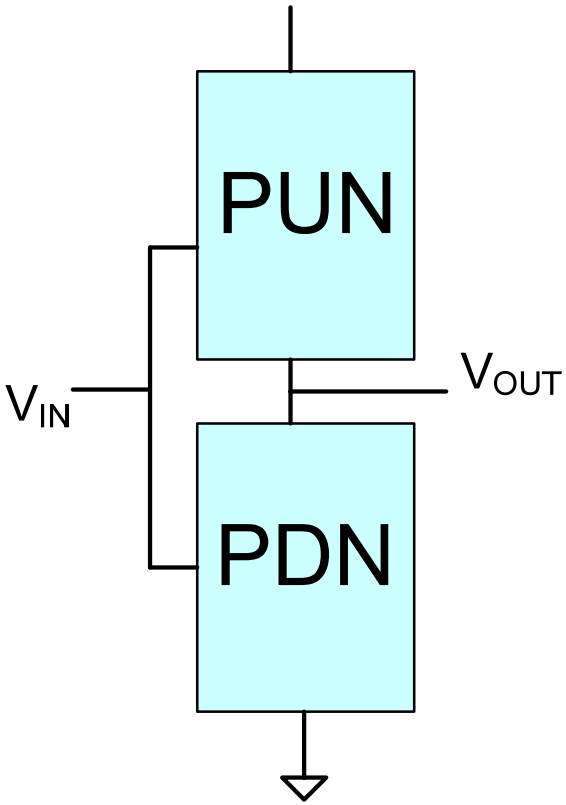
- Any number of inputs can be added to NAND or NOR Gates
- NAND and NOR Logic Families are Complete
- Can now build ANY combinational logic function !

Review from last time:

General Logic Family



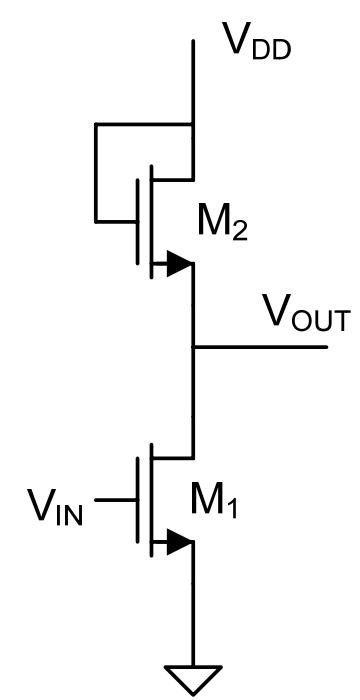
p-channel PUN
n-channel PDN



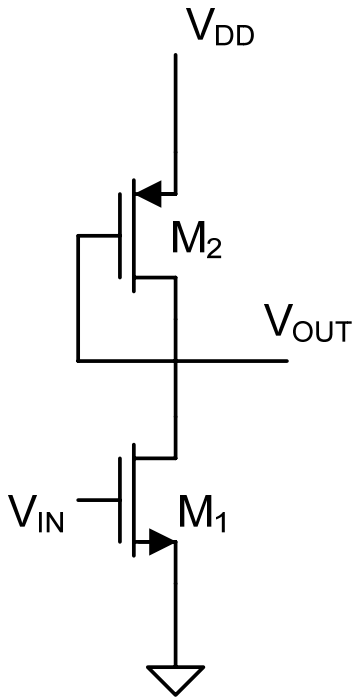
Arbitrary PUN
and PDN

Review from last time:

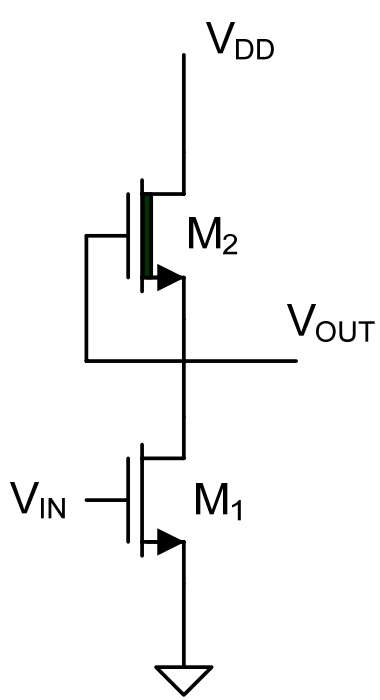
Other CMOS Logic Families



Enhancement
Load NMOS



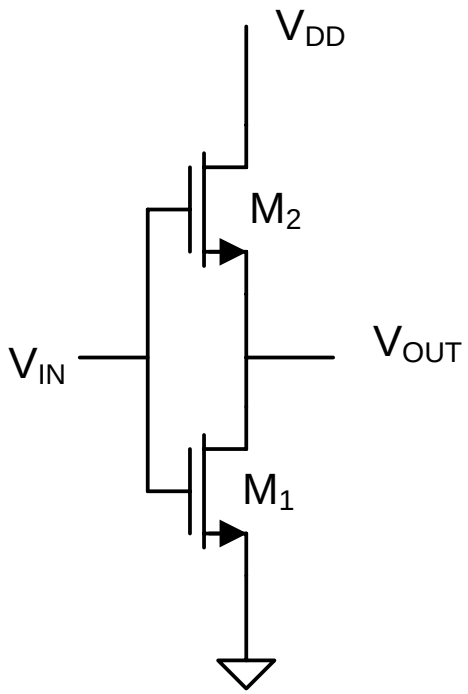
Enhancement Load
Pseudo-NMOS



Depletion
Load NMOS

Review from last time:

Static Power Dissipation in Static CMOS Family



When V_{OUT} is Low, I_{D1}=0

When V_{OUT} is High, I_{D2}=0

Thus, P_{STATIC}=0

This is a key property of the static CMOS Logic Family and is the major reason Static CMOS Logic is so dominant

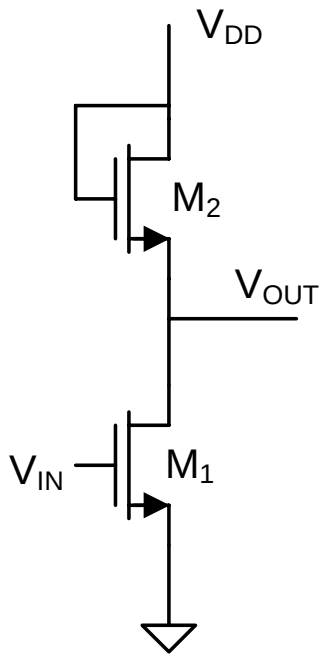
It can be shown that this zero static power dissipation property can be preserved if the PUN is comprised of n-channel devices, the PDN is comprised of n-channel devices and they are never both driven into the conducting states at the same time

Review from last time:

Static Power Dissipation in Ratio Logic Families

Example:

Assume V_{DD}=5V
V_T=1V, μC_{OX} =10^{-4}A/V^2, W_1/L_1=1 and M_2 sized so that $V_L=V_{Tn}$



Enhancement Load NMOS

P_L=(5V)(0.25mA)=1.25mW

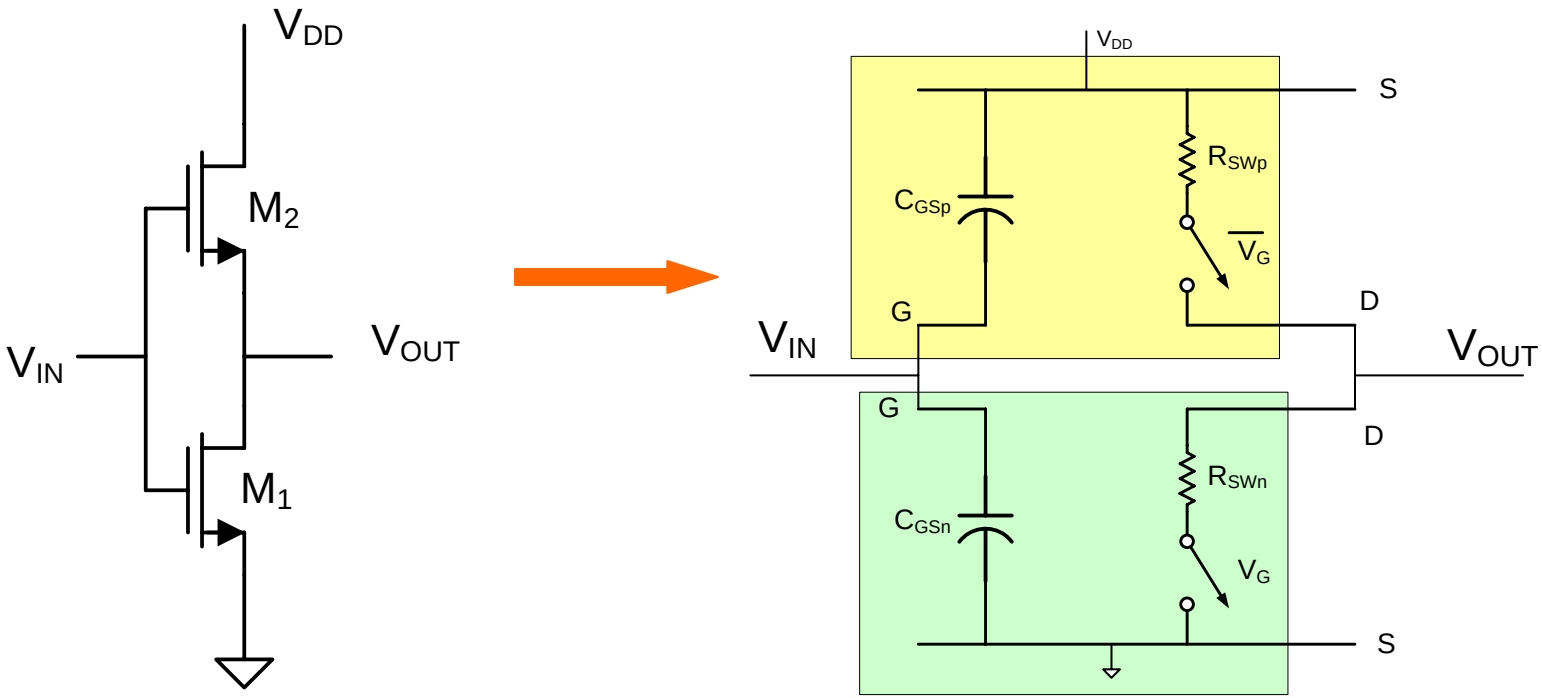
If a circuit has 100,000 gates and half of them are in the $V_{OUT}=V_L$ state, the static power dissipation will be

$$P_{STATIC} = \frac{1}{2}10^5 \bullet 1.25mW = \mathbf{62.5W}$$

This power dissipation is way too high and would be even larger in circuits with 100 million or more gates – the level of integration common in SoC circuits today

Review from last time:

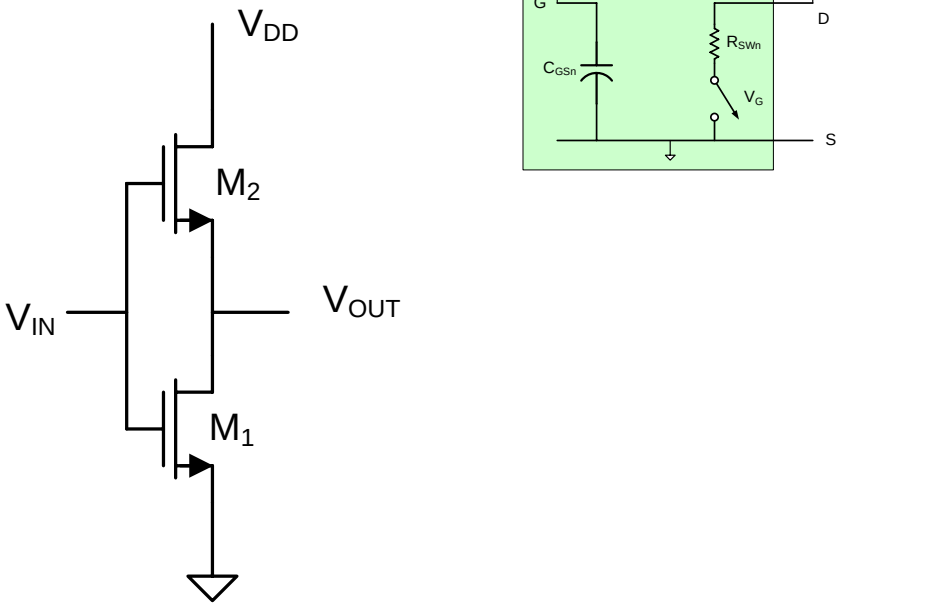
Propagation Delay in Static CMOS Family

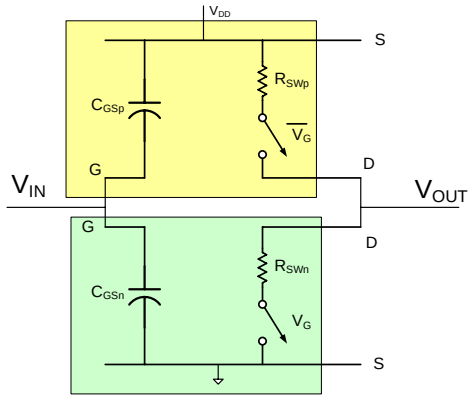


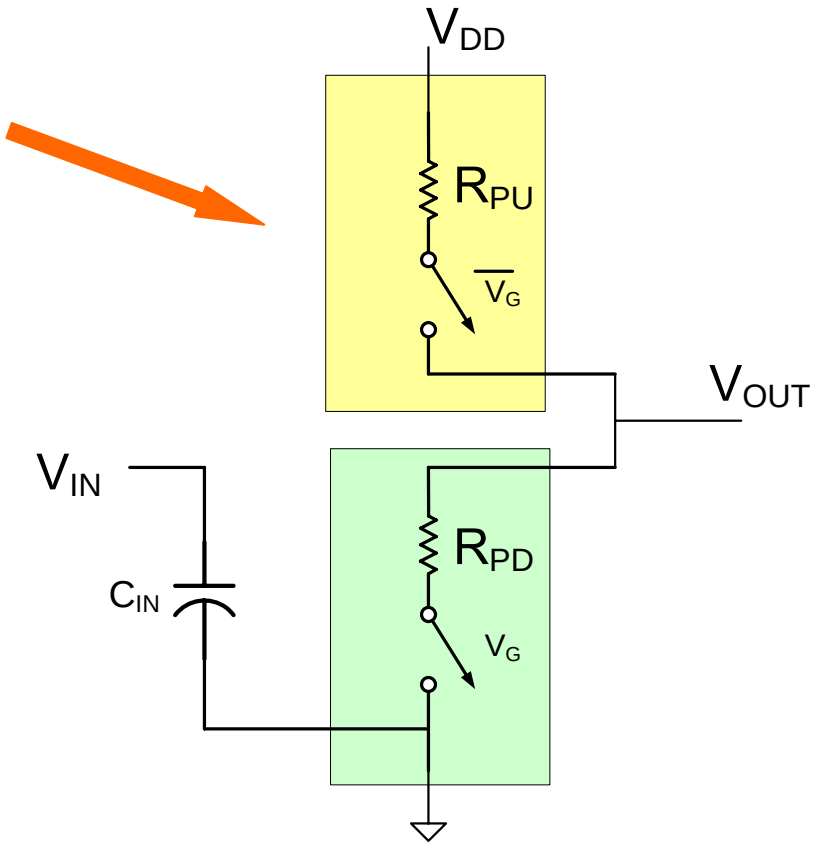
Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)

Review from last time:

Propagation Delay in Static CMOS Family

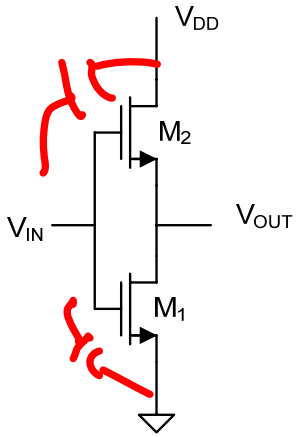


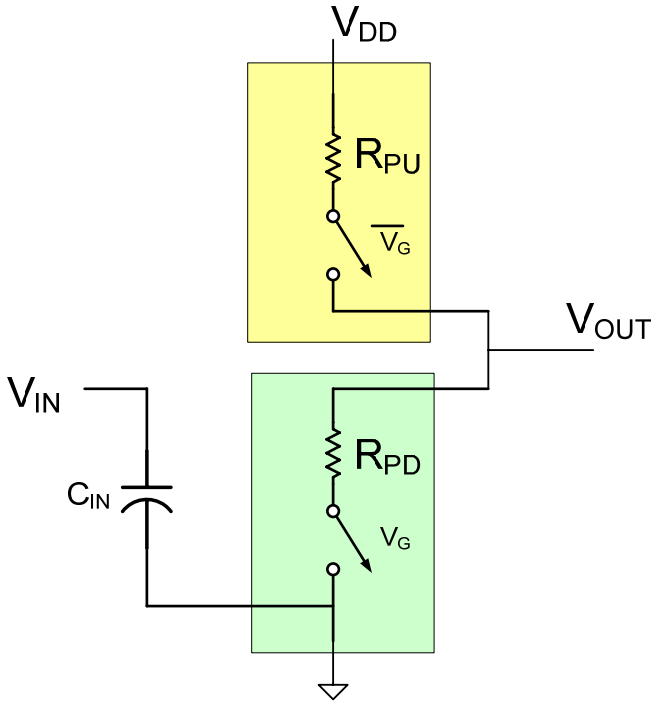




Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)

Propagation Delay in Static CMOS Family





Since operating in triode through most of transition:

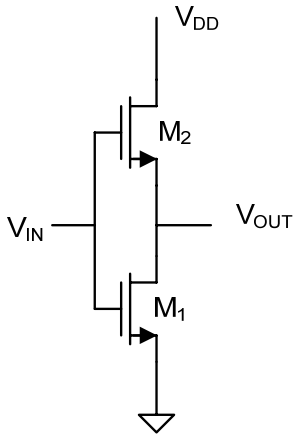
$$I_D \cong \frac{\mu C_{OX} W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \cong \frac{\mu C_{OX} W}{L}(V_{GS} - V_T)V_{DS}$$

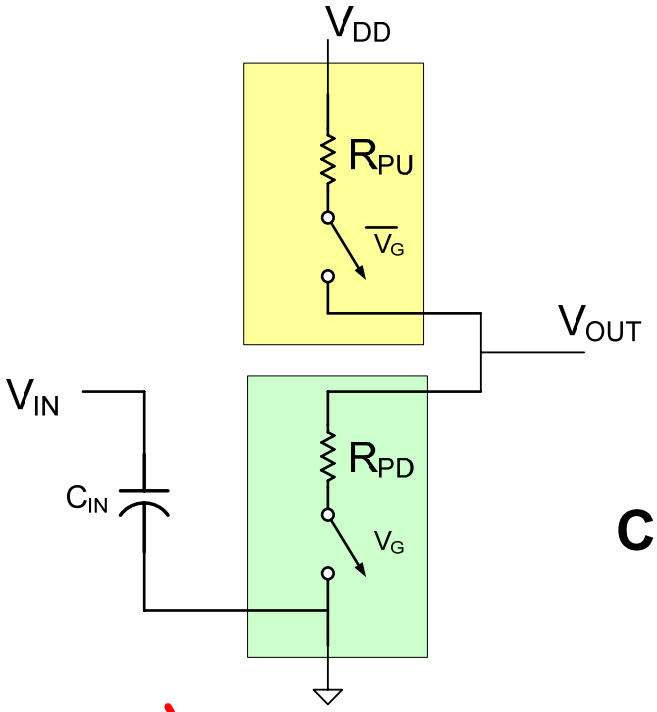
$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}$$

$$R_{PU} = \frac{I_D = \frac{\mu C_{OX} W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \cong \frac{\mu C_{OX} W}{L}(V_{GS} - V_T)V_{DS}}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}$$

$$C_{IN} = C_{OX}(W_1 L_1 + W_2 L_2)$$

Propagation Delay in Static CMOS Family





$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}$$

$$R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}$$

$$C_{IN} = C_{OX}(W_1 L_1 + W_2 L_2)$$

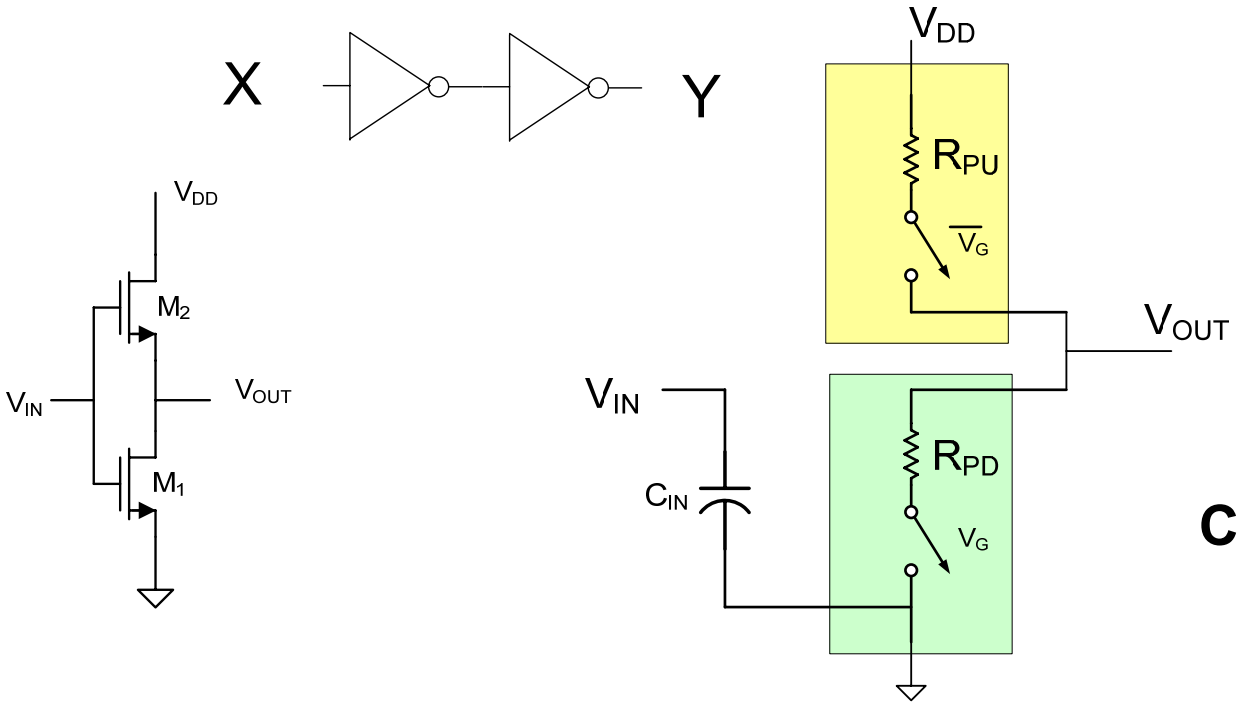
If $u_n C_{OX}=100\mu AV^{-2}$, $C_{OX}=4\ fF\mu^{-2}$, $V_{Tn}=V_{DD}/5$, $V_{TP}=-V_{DD}/5$, $\mu_n/\mu_p=3$, $L_1=W_1=L_{MIN}$, $L_2=W_2=L_{MIN}$, $L_{MIN}=0.5\mu$ and $V_{DD}=5V$

$$R_{PD} = \frac{1}{10^{-4} \bullet 0.8V_{DD}} = 2.5K\Omega$$

$$R_{PU} = \frac{1}{10^{-4} \bullet \frac{1}{3} \bullet 0.8V_{DD}} = 7.5K\Omega$$

$$C_{IN} = 4 \bullet 10^{-15} \bullet 2L_{MIN}^2 = 2fF$$

Propagation Delay in Static CMOS Family



$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}$$

$$R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}$$

$$C_{IN} = C_{OX}(W_1 L_1 + W_2 L_2)$$

If $u_n C_{OX}=100\mu AV^{-2}$, $C_{OX}=4\ fF\mu^{-2}$, $V_{Tn}=V_{DD}/5$, $V_{TP}=-V_{DD}/5$, $\mu_n/\mu_p=3$, $L_1=W_1=L_{MIN}$, $L_2=W_2=L_{MIN,}$ $L_{MIN}=0.5\mu$ and $V_{DD}=5V$

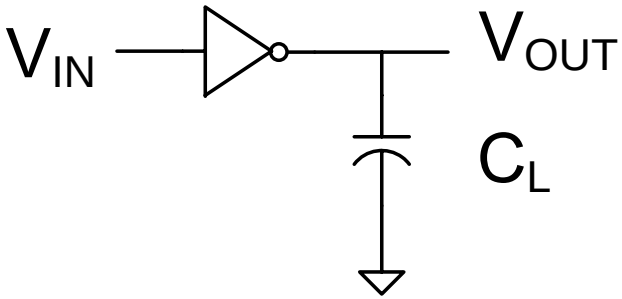
$$R_{PD} = \frac{1}{10^{-4} \bullet 0.8V_{DD}} = 2.5K\Omega$$

$$R_{PU} = \frac{1}{10^{-4} \bullet \frac{1}{3} \bullet 0.8V_{DD}} = 7.5K\Omega$$

$$C_{IN} = 4 \bullet 10^{-15} \bullet 2L_{MIN}^2 = 2fF$$

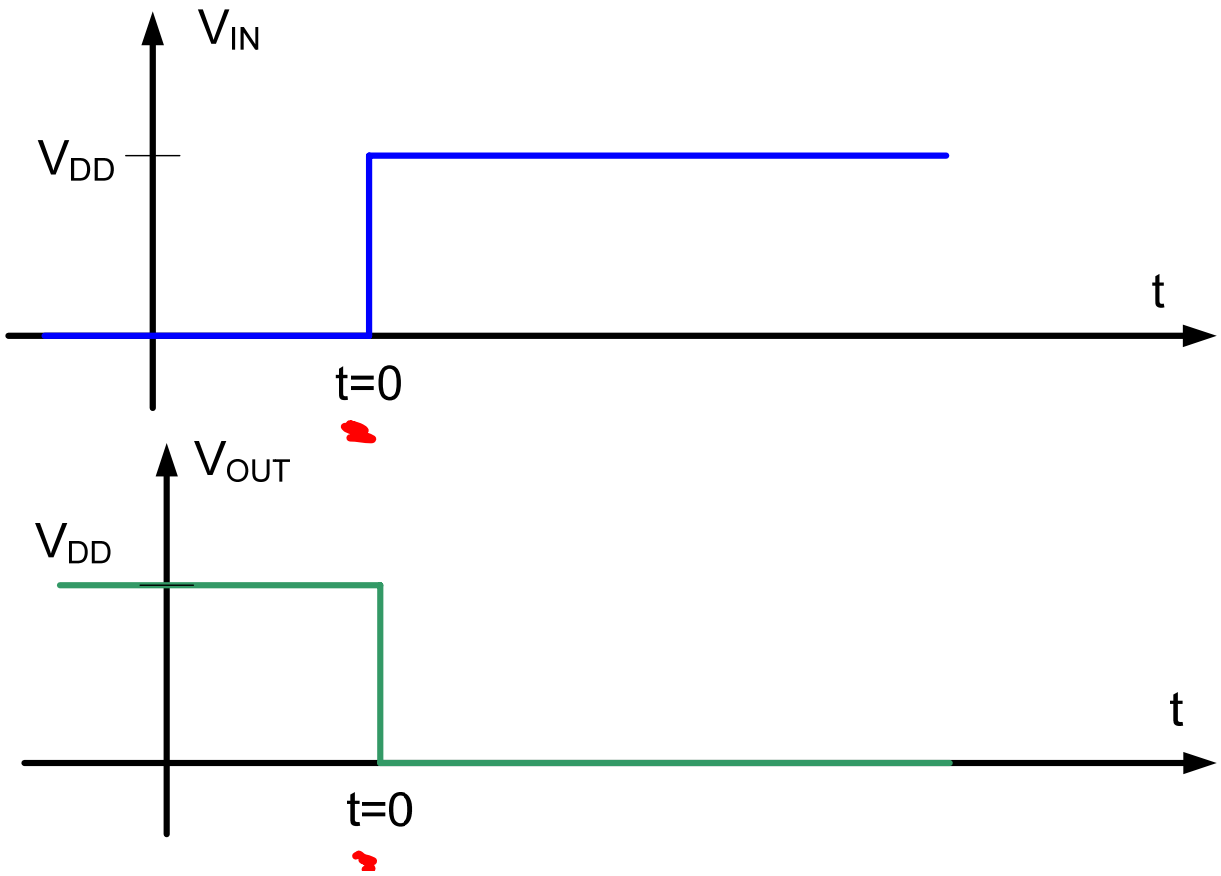
Propagation Delay in Static CMOS Family

Consider:



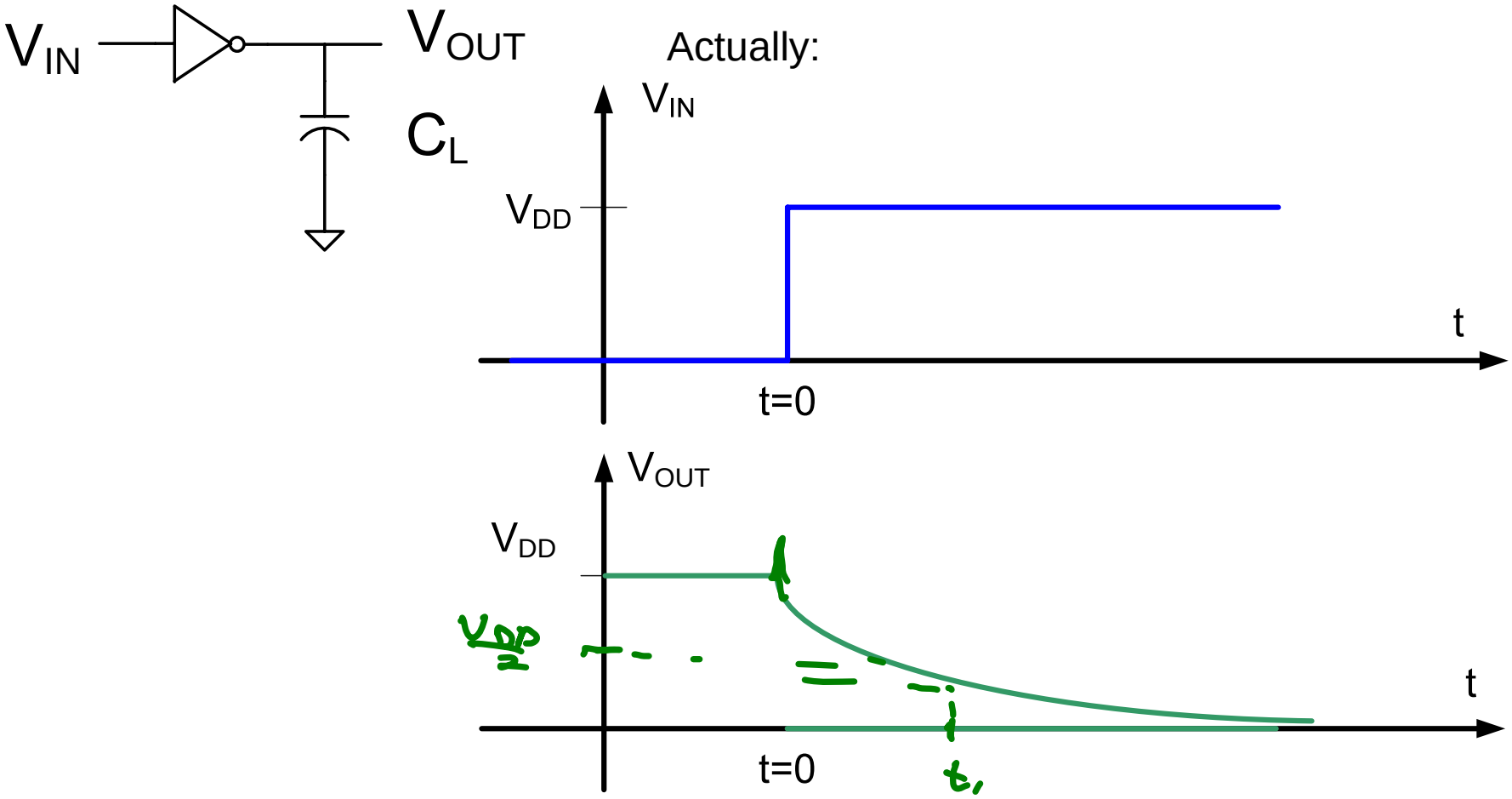
For HL output transition, C_L charged to V_{DD}

Ideally:



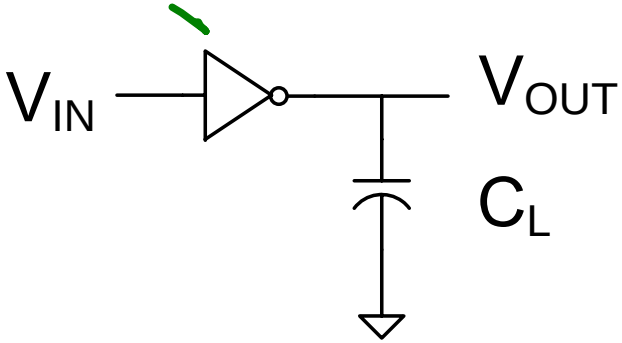
Propagation Delay in Static CMOS Family

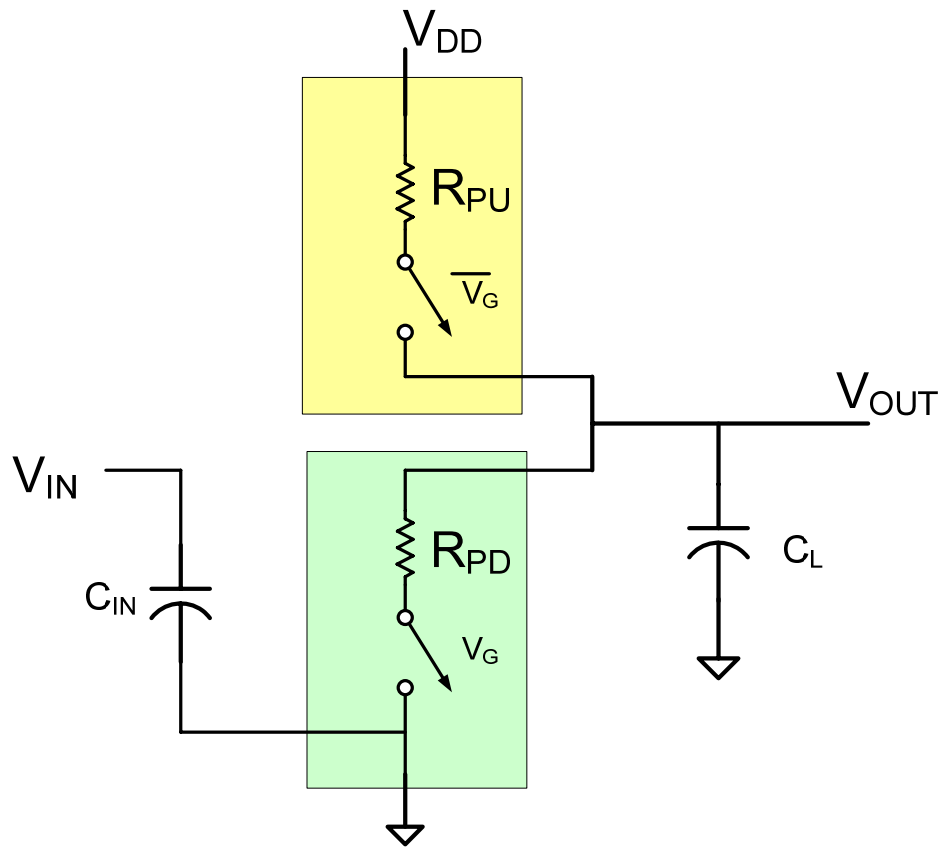
For HL output transition, C_L charged to V_{DD}



What is the transition time t_{HL} ?

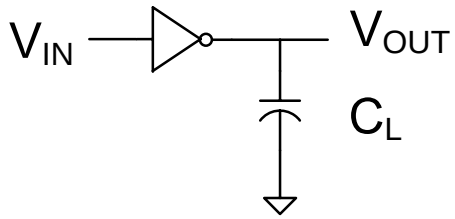
Propagation Delay in Static CMOS Family

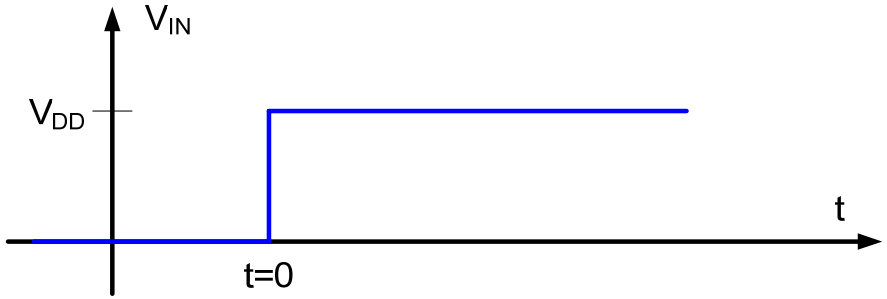


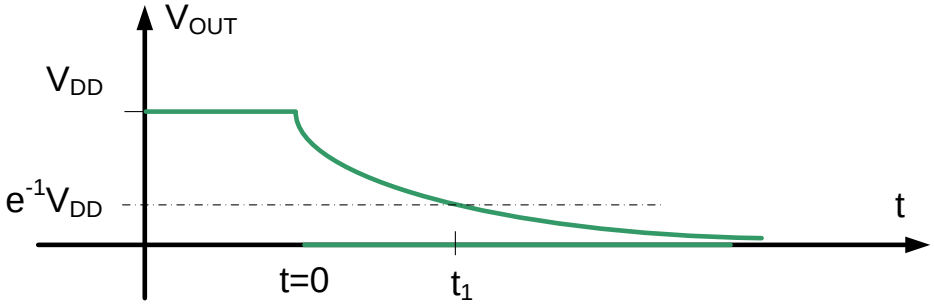


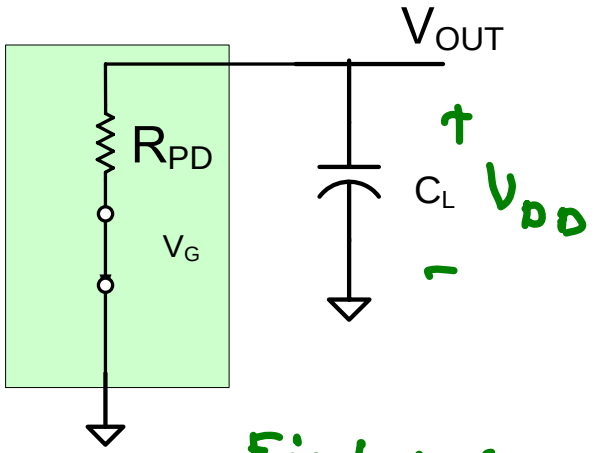
Propagation Delay in Static CMOS Family

For HL output transition, C_L charged to V_{DD}









First-order RC network

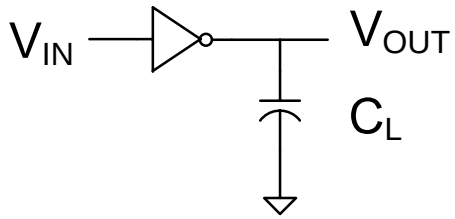
$$V_{OUT}(t) = F + (I - F)e^{\frac{-t}{\tau}} = 0 + (V_{DD} - 0)e^{-\frac{t}{R_{PD}C_L}}$$

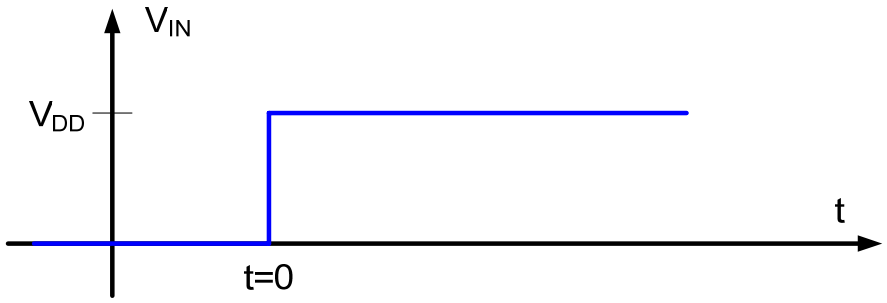
$$\frac{V_{DD}}{e} = V_{DD}e^{-\frac{t_1}{R_{PD}C_L}} \rightarrow t_1 = R_{PD}C_L$$

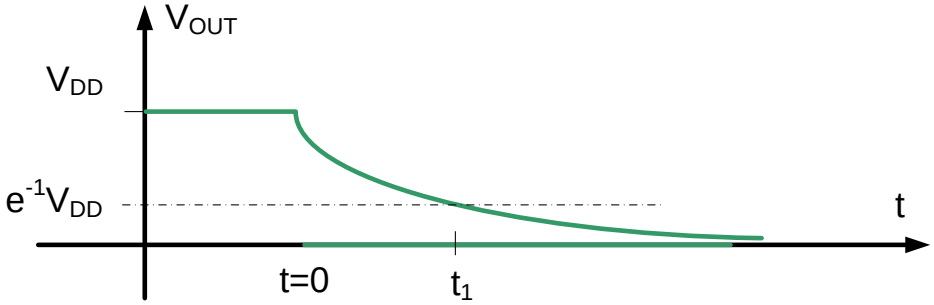
F = C
I = V_{DD}
$\tau = R_{PD} C_L$

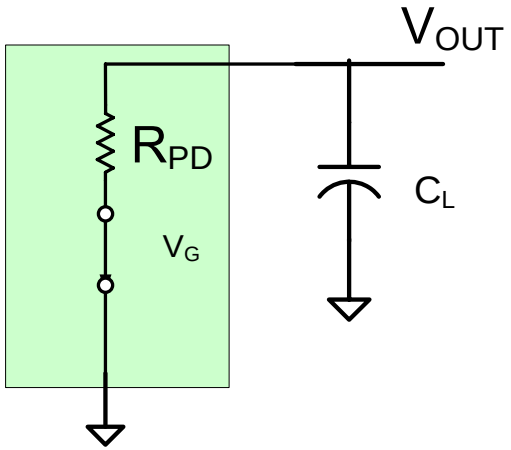
Propagation Delay in Static CMOS Family

For HL output transition, C_L charged to V_{DD}









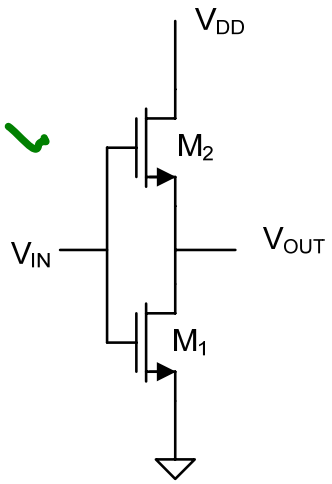
$t_{HL} = \theta R_{PD} C_L$

$\theta = 1$

$$t_{HL} \cong R_{PD} C_L$$

$$t_{LH} \cong R_{PU} C_L$$

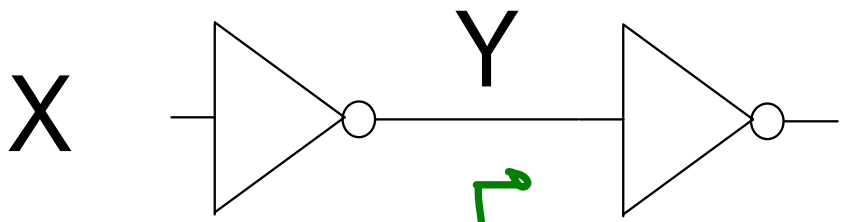
Propagation Delay in Static CMOS Family



$t_{HL} = ?$

$t_{LH} = ?$

all minimum sized



$C_L = C_{IN} = C_{ox}(W_1 L_1 + W_2 L_2)$

$\simeq 2\,fF$

$t_{HL} = R_{PD} C_L$

$= (2.5K)(2\,fF) = 5\,ps$

$t_{LH} = R_{PU} C_L$

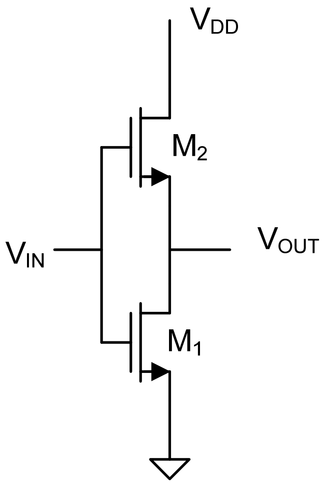
$= (7.5K)(2\,fF) = 15\,psec$

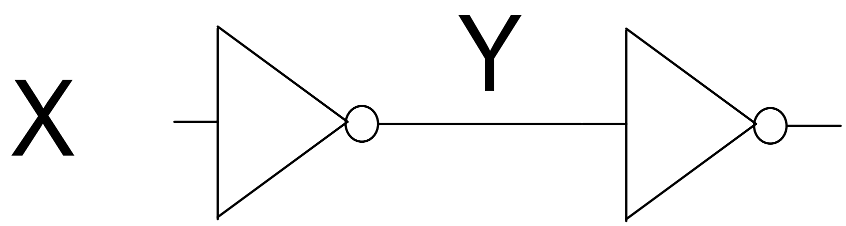
If

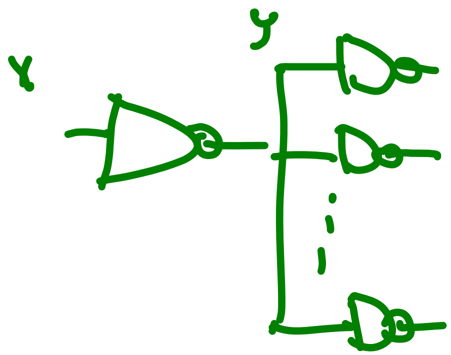
$t_{CL} = t_{HL} + t_{LH} = 20\,psec$

$\Rightarrow f_{CL} = 50\,GHz$

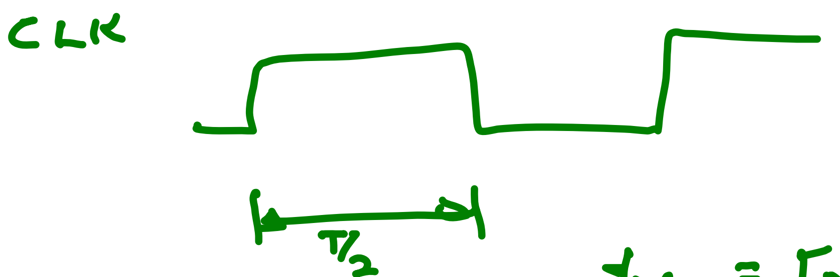
Propagation Delay in Static CMOS Family

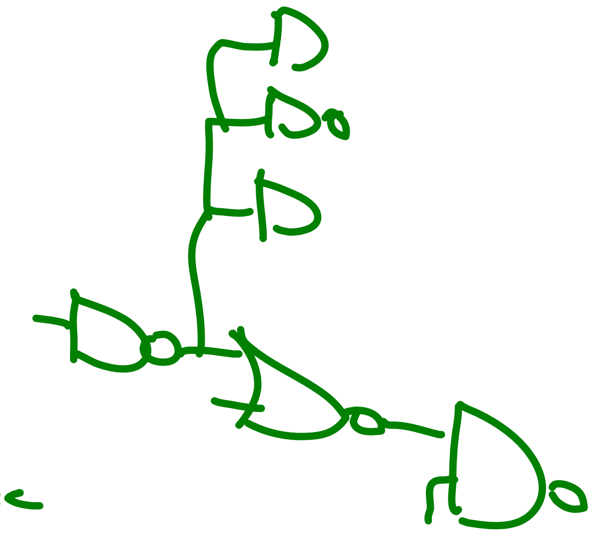






- driving multiple inputs slows down the logic

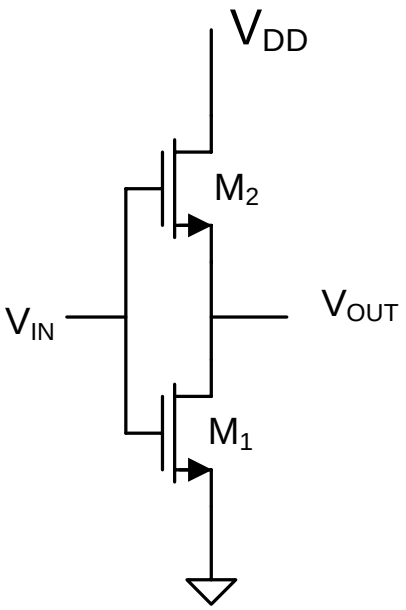




$t_{cz} = 5\,psec$

(8 levels of logic / 10 levels) ~ $t_{cz} \approx (80)(5\,psec) = 400psec$

Device Sizing



a) Minimum sized

b) Fix V_{TRIP} ($V_{DD}/2$)

c) Obtain equal rise & fall times

d) Minimum power dissipation

e) Minimize time required to drive a given load